CLAIMS

What is claimed is:

1. A method including:

detecting a power management event in a system; and

dynamically adjusting, in response to the power management event, the performance states of a plurality of system components including system buses.

2. The method of claim 1, wherein the power management event includes a change in the system power source from an AC outlet to a battery or vice versa.

3. The method of claim 1, wherein the system chipset drives the system buses.

4. The method of claim 1, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.

5. The method of claim 1, wherein the components include the memory subsystem, the graphics subsystem and the processor.

6. The method of claim 1, wherein the performance states are adjusted between a high level and a low level.

7. The method of claim 1, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.

8. The method of claim 7, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

9. The method of claim 1, wherein dynamically adjusting the performance states includes automatically placing the system in the deep sleep state (ACPI Specification C3 State) upon the occurrence of the power management event to adjust the performance states of the system components.

10. A method including:

detecting a power management event in a system; and

automatically placing the system in a low activity state, in response to the power management event,

adjusting the performance states of a plurality of system buses, and adjusting the performance states of a plurality of system components.

11. The method of claim 10, wherein the power management event includes a change in the system power source from an AC outlet to a battery or vice versa.

12. The method of claim 10, wherein the system chipset drives the system buses.

13. The method of claim 10, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.

14. The method of claim 10, wherein the components include the

processor, the memory subsystem and the graphics subsystem.

15. The method of claim 10, wherein the performance states are adjusted between a high level and low level.

16. The method of claim 10, wherein adjusting the performance state of the components includes adjusting the components supply voltages and clock frequencies.

17. The methods of claim 16, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

18. The method of claim 15, wherein the low activity state is the deep sleep state (ACPI Specification C3 State).

19. A system comprising:

a detector adapted to detect generation of a power management event; and

a controller to automatically adjust, in response to the power management event, the performance states of a plurality of system components including system buses.

20. The system of claim 19, wherein the power of management event includes a change in the system power source from an AC outlet to a battery or vice versa.

21. The system of claim 19, wherein the system chipset drives the system buses.

22. The system of claim 19, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.

23. The system of claim 19, wherein the components include the processor, the memory subsystem and the graphics subsystem.

Sub A1

24. The system of claim 19, wherein the performance states are adjusted between a high level and a low level.

25. The system of claim 19, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.

26. The system of claim 25, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

27. The system of claim 19, wherein the low activity state is the deep sleep state (ACPI Specification C3 State).

28. An apparatus comprising:

a detector adapted to detect generation of power management event; and

a controller to automatically adjust, in response to the power management event, the performance states of a plurality of system components including system buses.

29. The apparatus of claim 28, wherein the power of management

event includes a change in the system power source from an AC outlet to a battery or vice versa.

30. The apparatus of claim 28, wherein the system chipset drives the system buses.

Sub A1

31. The apparatus of claim 28, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.

32. The apparatus of claim 28, wherein the components include the processor, the memory subsystem and the graphics subsystem.

33. The apparatus of claim 28, wherein the performance states are adjusted between a high level and a low level.

34. The apparatus of claim 28, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.

35. The apparatus of claim 34, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

36. The apparatus of claim 28, wherein the low activity state is the deep sleep state (ACPI Specification C3 State).

37. A computer-readable medium having stored thereon a set of instructions to translate instructions, the set instructions, which when

executed by a processor, cause the processor to perform a method comprising:

detecting a power management event in a system; and

dynamically adjusting, in response to the power management event, the performance states of a plurality of system components including system buses.

Sub A1

38. The computer-readable medium of claim 37, wherein the power management event includes a change in the system power source from an AC outlet to a battery or vice versa.

39. The computer-readable medium of claim 37, wherein the chipset drives the system buses.

40. The computer-readable medium of claim 37, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.

41. The computer-readable medium of claim 37, wherein the components include the memory subsystem, the graphics subsystem and the processor.

42. The computer-readable medium of claim 37, wherein the performance states are adjusted between a high level and a low level.

43. The computer-readable medium of claim 37, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.

44. The computer-readable medium of claim 43, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

45. The computer-readable medium of claim 37, wherein dynamically adjusting the performance states includes automatically placing the system in the deep sleep state (ACPI Specification C3 State) upon the occurrence of the power management event to adjust the performance states of the system components.